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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,881	03/31/2004	Masahiro Koyama	500.37600CX1	4560

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EXAMINER	
LAFORGIA, CHRISTIAN A	

ART UNIT	PAPER NUMBER
2139	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,881	KOYAMA ET AL.	
	Examiner	Art Unit	
	Christian LaForgia	2139	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/398,776.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment of 20 February 2008 has been noted and made of record.

2. Claims 1-8 and 17 have been presented for examination.

3. Claims 9-16 and 18-21 have been cancelled as per Applicant's request.

Response to Arguments

4. Applicant's arguments, see pages 7 and 8, filed 20 February 2008, with respect to the 35 U.S.C. 112, 2nd paragraph rejections have been fully considered and are persuasive. The 35 U.S.C. 112, 2nd paragraph rejection of claim 17 has been withdrawn. The rejection of claims 18-21 is moot since they have been cancelled.

5. The 35 U.S.C. 101 rejection of claims 15, 16, and 21 is moot since they have been cancelled.

6. Applicant's arguments with respect to claims 1-8 and 17 have been considered but are moot in view of the new grounds of rejection set forth below.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 3-5, and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 5,978,844 to Tsuchiya et al., hereinafter Tsuchiya.

9. The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

10. As per claim 1, Tsuchiya teaches a decentralized control system, comprising:

a plurality of processors (Figure 1 [blocks 1, 2, 3, 4]);

a plurality of devices controlled by said plurality of processors (Figure 1 [blocks 26-29, 52-55, 64-67, 74-77], i.e. transmitter units, statistic units, and transceiver units); and,

at least one information transmission path for communicating control of information between the plurality of processors and for communicating input/output information between said plurality of processors and the devices (Figure 1 [element 91], i.e. message bus);

wherein each of the plurality of processors comprises:

processor detecting means for detecting a connection state of each of the plurality of processors with respect to the information transmission path, said connection state being represented by an ID of each of said processors (Figure 1 [elements 52-55], column 2, lines 18-25, column 2, lines 36-44);

wherein said processor detecting means generates a list of available processors (Figure 1 [elements 60-63], column 7, line 44 to column 8, line 5),

wherein at least one of said plurality of processors comprises:

program block assigning means for assigning, based on the detected connection state detected by said processor detecting means, a plurality of mutually concurrently executable program blocks to control the device to each of said plurality of processors, respectively (Figure 1 [elements 40-43], column 5, lines 27-54),

wherein said program block assigning means divides a program for controlling said devices into said mutually concurrently executable plurality of blocks allowing uniform assignment of a processing load to the processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks, generates an assignment list, and distributes the assignment list and said mutually concurrently executable plurality of blocks to said processors (Figure 1 [element 82], column 2, line 33 to column 3, line 3, column 5, lines 27-54); and

a program storage means for storing a relevant one of the plurality of mutually concurrently executable program blocks at each of the plurality of processors, each of the plurality of processors executing the stored relevant program blocks, respectively (Figure 1 [elements 69-72], column 10, lines 23-38, i.e. data buffers) and,

wherein each of said plurality of processors distributes said mutually concurrently executable plurality of blocks and said assignment list, and executes the program blocks based on said assignment list (column 2, line 33 to column 3, line 3, column 5, lines 27-54).

11. Regarding claim 3, Tsuchiya teaches each of the plurality of processors detects by the processor detecting means thereof available processors connected to the information

transmission path (Figure 1 [elements 52-55], column 2, lines 18-25, column 2, lines 36-44) and assigns by the program assigning means thereof processing of the program blocks respectively to the plurality of processors (Figure 1 [element 82], column 2, line 33 to column 3, line 3, column 5, lines 27-54).

12. Regarding claim 4, Tsuchiya teaches wherein each one of the plurality of processors generates by the program block assigning means an allocation table in which the program blocks are subdivided into several groups to be respectively assigned to the plurality of processors to possibly uniformly assign a processing load to the processors in accordance with an average number of steps or an average processing time for one cycle of each of the plural program blocks and sends the table to each of the plurality of processors together with all the program blocks (Figure 1 [element 82], column 2, line 33 to column 3, line 3, column 5, lines 27-54, column 7, line 44 to column 8, line 5, column 8, lines 42-67, column 10, lines 23-38).

13. With regards to claim 5, Tsuchiya teaches either one of the plurality of processors subdivides by the program block assigning means the program blocks into program block sets each including several ones of the program blocks and assigns the program block sets respectively to the plurality of processors to possibly uniformly assign a processing load to the processors in accordance with an average number of steps or an average processing time for one cycle of each of the plurality of program blocks and sends the program block sets respectively to the plurality of processors (Figure 1 [element 82], column 2, line 33 to column 3, line 3, column

5, lines 27-54, column 7, line 44 to column 8, line 5, column 8, lines 42-67, column 10, lines 23-38).

14. Regarding claim 6, Tsuchiya teaches means for multicasting via the information transmission path a connection state of its own processor with respect to the information transmission path, the means including the processor detecting means (Figure 1 [elements 21-24], column 7, lines 44-67);

a means for generating, in accordance with connection states sent via the information transmission path from other processors, a list of available processors connected to the information transmission path (Figure 1 [elements 52-55], column 2, lines 18-25, column 2, lines 36-44).

15. Regarding claim 7, Tsuchiya teaches that either one of the plurality of processors detects by the processor detecting means, when the connection state of either one of said plurality of processors is changed in the decentralized control system or either one of the plurality of processors fails when the decentralized control system is in operation, available processors and assigns by the program block assigning means processing of the plural program blocks to the available processors (Figure 1 [elements 52-55, 82], column 2, lines 18-25, column 2, lines 36-44, column 5, lines 27-54, column 7, line 44 to column 8, line 5, column 8, lines 42-67, column 10, lines 23-38).

16. Regarding claim 17, Tsuchiya teaches wherein each of numbers of instructions of the mutually concurrently executable program blocks to be assigned to each of the processors are made substantially equal (Figure 1 [element 82], column 2, lines 49-56).

Claim Rejections - 35 USC § 103

17. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

18. Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being obvious over Tsuchiya in view of United States Patent No. 5,592,671 to Hirayama, hereinafter Hirayama.

19. Regarding claim 2, Tsuchiya does not teach a particular processor selected in accordance with the priority level from available processors detected by the processor detecting means assigns by the program assigning means processing of the program blocks respectively to said plurality of processors;

the plurality of processors are assigned with priority levels beforehand.

20. Hirayama teaches a particular processor selected in accordance with the priority level from available processors detected by the processor detecting means assigns by the program assigning means processing of the program blocks respectively to said plurality of processors (Figures 1, 5, 8; column 3, lines 17-34; column 3, lines 43-57);

the plurality of processors are assigned with priority levels beforehand (column 3, lines 27-30). Tsuchiya suggests in column 5 that the plurality of processors rank differently amongst themselves, particularly amongst processing power and speed. Furthermore, Tsuchiya discloses running the divisible task on slower machines, that will take longer and cost less or executing the divisible task on faster processors, costing more, but taking less time in columns 10 and 11.

Therefore it would have been obvious to one of ordinary skill in the art, with a working knowledge of Hirayama, at the time the invention was made to assign a priority level to each of the plurality of processors.

21. Regarding claim 8, Tsuchiya does not the information transmission path includes two channels, namely, a control information transmission path for communicating the control information and an input/output information transmission path to communicate the input/output information.

22. Hirayama teaches the information transmission path includes two channels, namely, a control information transmission path for communicating the control information and an input/output information transmission path to communicate the input/output information (Figures 5 [blocks 53, 520, 521, 522, 52n], 7 [blocks 73, 702, 712, 722, 7m2]; column 4, line 64 to column 5, line 9; column 6, line 54 to column 7, line 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have two channels, an I/O path and a control path, in the system of Saito. One would be motivated to include these multiple channels for redundancy purposes. In the case that a processor fails and control has to be transferred to another processor, the other processors can communicate without putting traffic on the I/O path and disrupting that path. Likewise, if a processor fails, the information on the I/O path can just be forwarded to the appropriate processor without having to retransmit the information several times until it finds the appropriate processor.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

24. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian LaForgia whose telephone number is (571)272-3792. The examiner can normally be reached on Monday thru Thursday 7-5.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kristine L. Kincaid can be reached on (571) 272-4063. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Christian LaForgia/
Primary Examiner, Art Unit 2139

clf